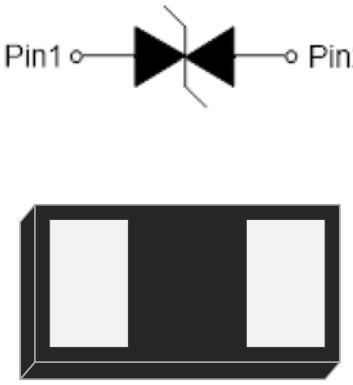
RoHS
COMPLIANT

ESDULC3V6LZB

1-Line, Bi-directional, Transient Voltage Suppressor



DFN0603-2L

Features

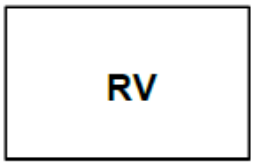
- Stand-off voltage: 3.3V Max
- Transient protection for each line according to
  IEC61000-4-2(ESD): 20 kV (contact)
  IEC61000-4-5(surge): 3 A (8/20μs)
- Low leakage current
- Low clamping voltage
- Low clamping voltage:
- RoHS Compliant

Applications

- Cellular Handsets and Accessories
- Display Ports
- MDDI Ports
- USB Ports
- Digital Visual Interface (DVI)
- PCI Express and Serial SATA Ports

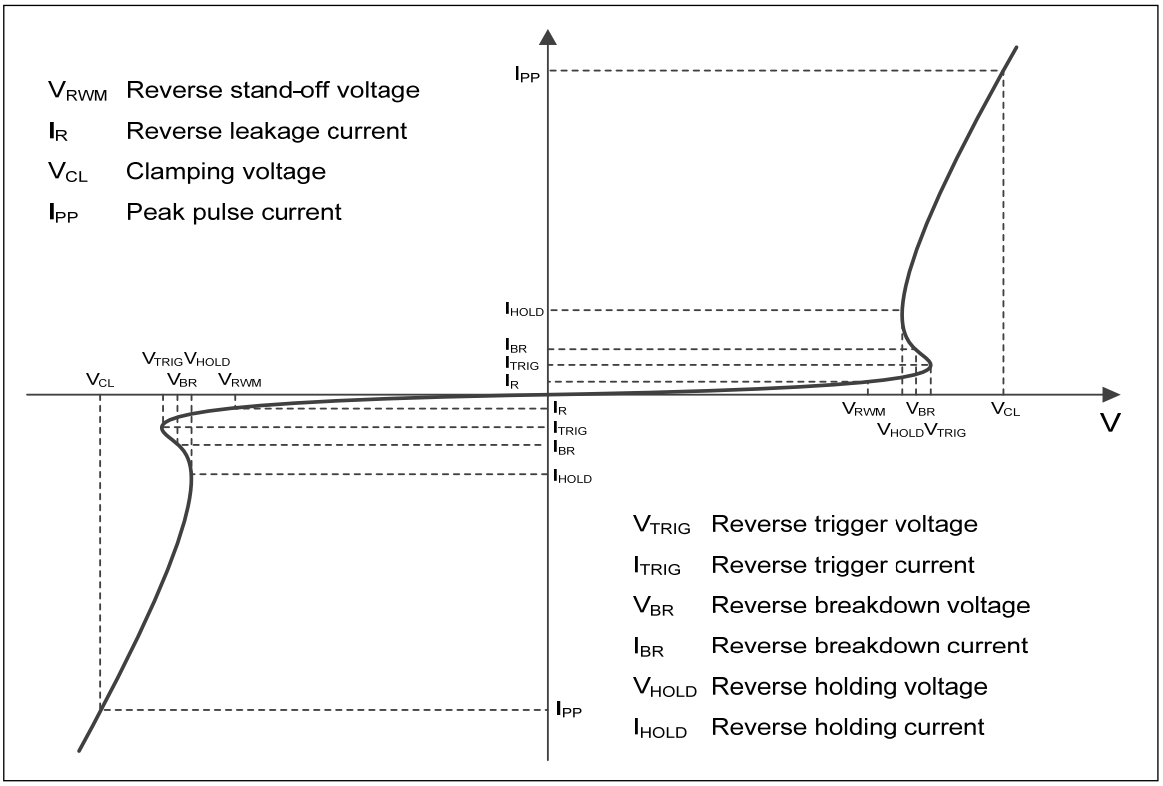
Mechanical Data

- Package: DFN0603-2L
- Case Material: “Green” Molding Compound
- Moisture Sensitivity: Level 3 per J-STD-020
- Marking Information: See Below



RV = Device Marking Code

■Definitions of electrical characteristics



■Maximum Ratings

PARAMETER	SYMBOL	LIMITS	UNIT
Peak pulse power (t_p = 8/20μs)	P_{pk}	45	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	3	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±20	kV
ESD according to IEC61000-4-2 contact discharge		±20	
Junction temperature	T_J	-55~125	ºC
Storage temperature	T_{STG}	-55~150	ºC

■Electrical Characteristics（T_a=25℃ Unless otherwise specified）

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V_{RWM}	V			3.3	3.6
Reverse leakage current	I_R	uA	V_{RWM} = 3.3V			0.2
Reverse breakdown voltage	V_{BR}	V	I_{BR} = 1mA	5		
Clamping voltage [1)]	V_{CL}	V	I_{PP} = 1A, t_p = 0.2/100ns(TLP)			11
Clamping voltage [1)]	V_{CL}	V	I_{PP} = 3A, t_p = 0.2/100ns(TLP)			15
Junction capacitance	C_J	pF	V_R = 0V, f = 1MHz		0.15	0.25

Notes:
(1). Non-repetitive current pulse, according to IEC61000-4-5.

■Ordering Information (Example)

PREFERED P/N	PACKING CODE	UNIT WEIGHT(mg)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
ESDULC3V6LZB	F1	Approximate 0.18	10000	100000	400000	7” reel

■ Characteristics (Typical)

Fig.1 8/20μs waveform per IEC61000-4-5

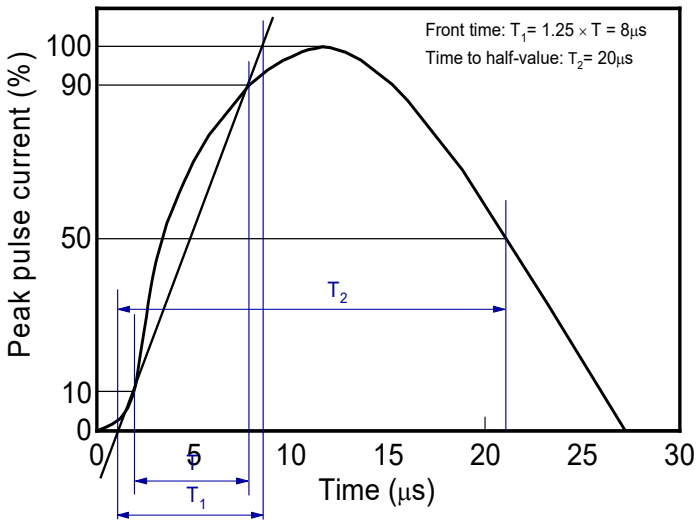


Fig.2 Contact discharge current waveform per IEC61000-4-2

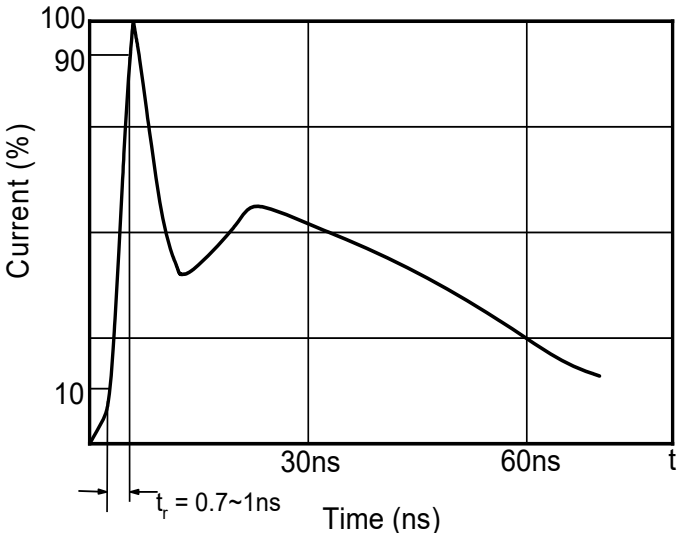


Fig.3 Clamping voltage vs. Peak pulse current

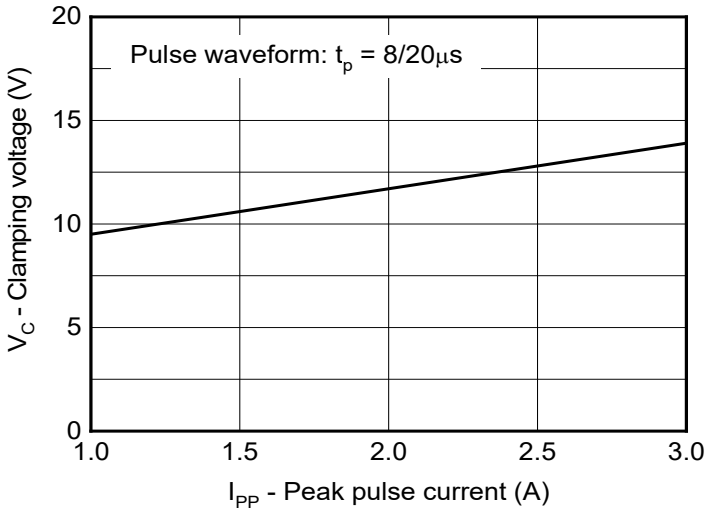


Fig.4 Capacitance vs. Reverse voltage

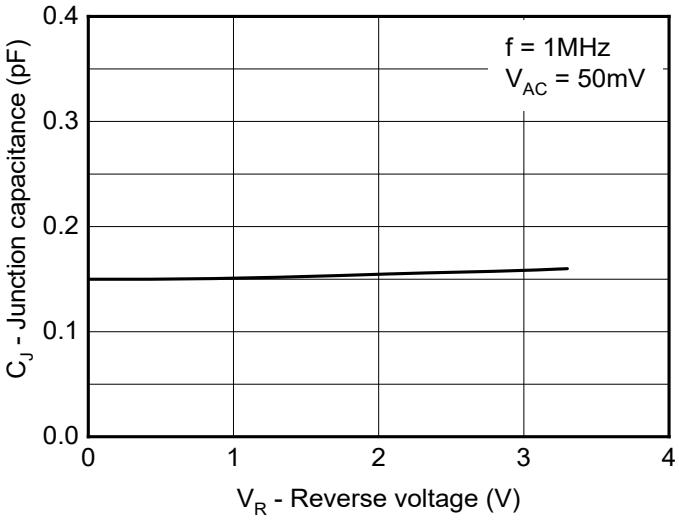


Fig.5 Non-repetitive peak pulse power vs. Pulse time

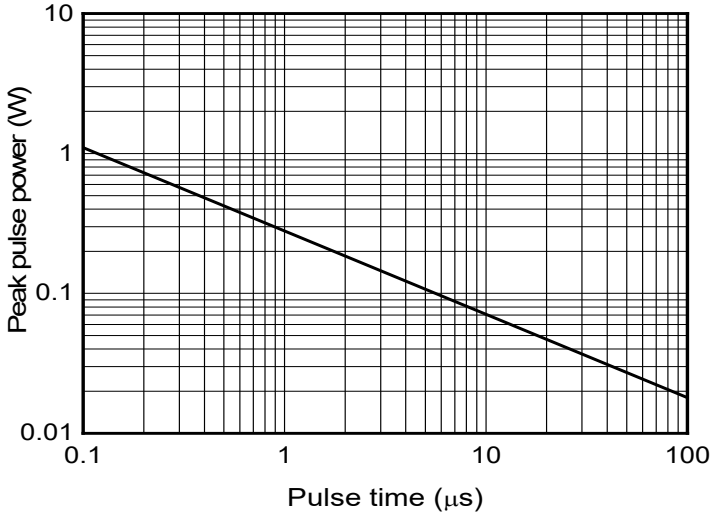


Fig.6 Power derating vs. Ambient temperature

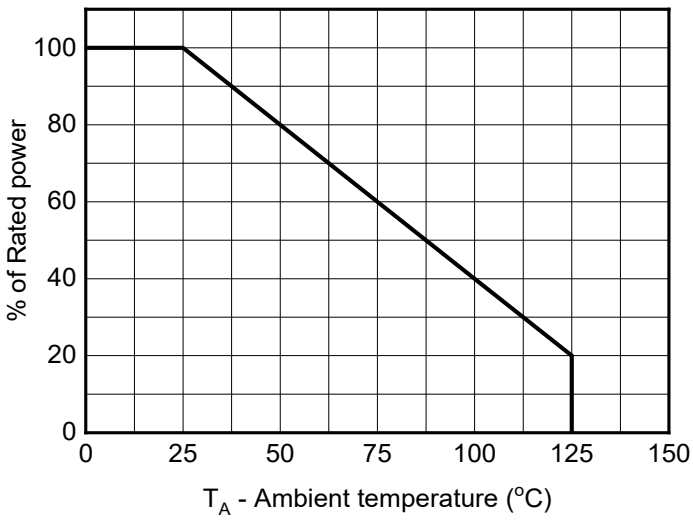
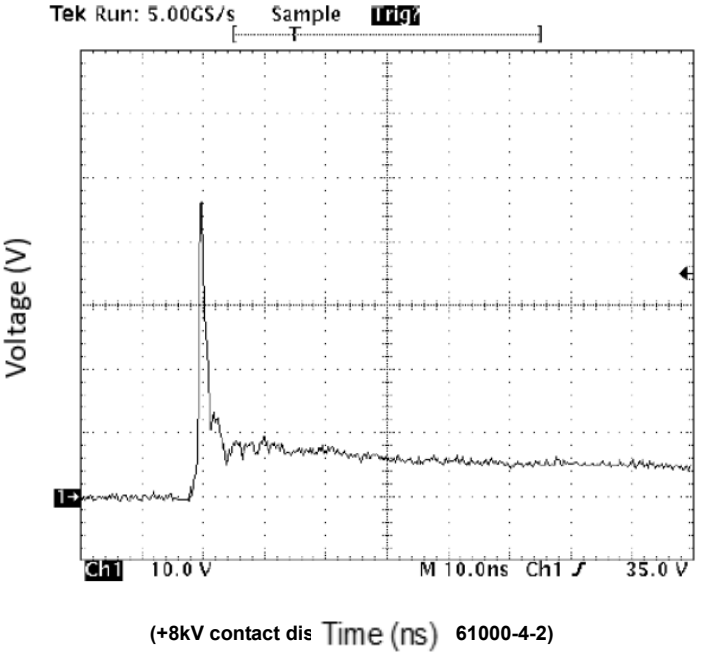
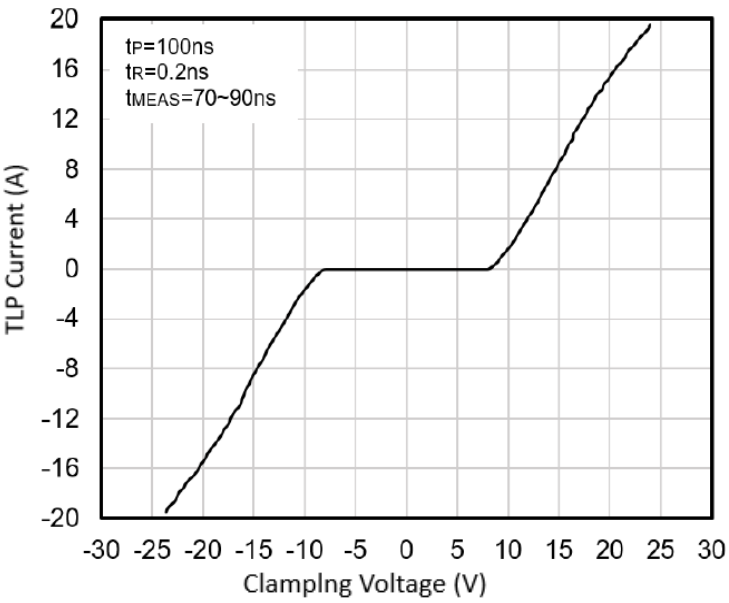


Fig.7 ESD clamping

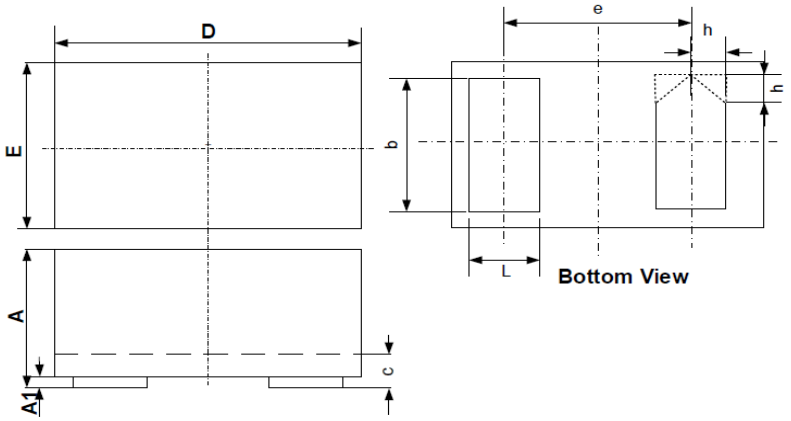
Fig.8 TLP Measurment





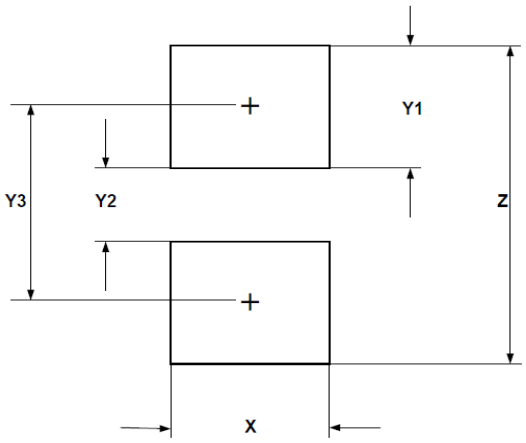
■ Outline

Dimensions



SYM	DIMENSIONS		
	MILLIMETERS		
	MIN	NOM	MAX
A	0.230		0.330
A1	0.000	0.020	0.050
b	0.215	0.245	0.275
c	0.120	0.150	0.180
D	0.550	0.600	0.650
e	0.355 BSC		
E	0.250	0.300	0.350
L	0.160	0.190	0.220
h	0.079 BSC		

■ Recommended PCB Layout



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X	0.30	0.012
Y1	0.25	0.010
Y2	0.15	0.006
Y3	0.40	0.016
Z	0.65	0.026

Unit:mm

Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met

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